(gdb) print config

$3 = (const gpgpu\_sim\_config &) @0x7ffff7dd35a0: {<power\_config> = {

g\_power\_config\_name = "gpuwattch\_gtx480.xml",  
 m\_valid = true,  
 g\_power\_simulation\_enabled = true

g\_power\_trace\_enabled = true,  
g\_steady\_power\_levels\_enabled = true,  
g\_power\_per\_cycle\_dump = true,  
g\_power\_simulator\_debug = false,  
g\_power\_filename = 0x62b0b0 "gpgpusim\_power\_report\_\_Wed-Feb-13-13-30-03-2019.log",  
 g\_power\_trace\_filename = 0x62bb10 "gpgpusim\_power\_trace\_report\_\_Wed-Feb-13-13-30-03-2019.log.gz",

g\_metric\_trace\_filename = 0x6234f0 "gpgpusim\_metric\_trace\_report\_\_Wed-Feb-13-13-30-03-2019.log.gz",

g\_steady\_state\_tracking\_filename = 0x620d00 "gpgpusim\_steady\_state\_tracking\_report\_\_Wed-Feb-13-13-30-03-2019.log.gz",  
 g\_power\_trace\_zlevel = 6,

gpu\_steady\_state\_definition = 0x7ffff7a7c2ee "8:4",  
 gpu\_steady\_power\_deviation = 8,  
 gpu\_steady\_min\_period = 4,  
 g\_use\_nonlinear\_model = false,  
 gpu\_nonlinear\_model\_config = 0x0,

gpu\_idle\_core\_power = 0,  
 gpu\_min\_inc\_per\_active\_sm = 0},  
 <gpgpu\_functional\_sim\_config> = {m\_ptx\_convert\_to\_ptxplus = 0,  
 m\_ptx\_use\_cuobjdump = 1,  
 m\_experimental\_lib\_support = 0,

m\_ptx\_force\_max\_capability = 61,  
 g\_ptx\_inst\_debug\_to\_file = 1,  
 g\_ptx\_inst\_debug\_file = 0x7ffff7a91a4c "inst\_debug.txt",  
 g\_ptx\_inst\_debug\_thread\_uid = 1,  
 m\_texcache\_linesize = 128},

m\_valid = true,  
 m\_shader\_config = {<core\_config> = {\_vptr.core\_config = 0x7ffff7da18c8 <vtable for shader\_core\_config+16>,  
 m\_valid = true,  
 warp\_size = 32,  
 gpgpu\_coalesce\_arch = 13,

shmem\_limited\_broadcast = false,  
 static WORD\_SIZE = 4,  
 num\_shmem\_bank = 32,  
 mem\_warp\_parts = 1,  
 gpgpu\_shmem\_size = 16384,  
 gpgpu\_shmem\_sizeDefault = 49152,

gpgpu\_shmem\_sizePrefL1 = 16384,  
 gpgpu\_shmem\_sizePrefShared = 16384,  
 gpgpu\_cache\_texl1\_linesize = 128,  
 gpgpu\_cache\_constl1\_linesize = 64,  
 gpgpu\_max\_insn\_issue\_per\_warp = 0},

gpgpu\_shader\_core\_pipeline\_opt = 0x62c1e0 "1536:32",  
 gpgpu\_perfect\_mem = false,  
 gpgpu\_clock\_gated\_reg\_file = false,  
 gpgpu\_clock\_gated\_lanes = false,  
 model = POST\_DOMINATOR,

n\_thread\_per\_shader = 1536,  
 n\_regfile\_gating\_group = 4,  
 max\_warps\_per\_shader = 48,  
 max\_cta\_per\_core = 8,  
 max\_barriers\_per\_cta = 16,  
 gpgpu\_scheduler\_string = 0x62ba00 "gto",

pipeline\_widths\_string = 0x62b860 "2,  
1,  
1,  
2,  
1,  
1,  
2",  
 pipe\_widths = {2,  
 1,  
 1,  
 2,  
 1,  
 1,  
 2},  
 m\_L1I\_config = {\_vptr.cache\_config = 0x7ffff7da18e0 <vtable for cache\_config+16>,

m\_config\_string = 0x62ba20 "4:128:4,  
L:R:f:N:L,  
A:2:32,  
4",  
 m\_config\_stringPrefL1 = 0x0,  
 m\_config\_stringPrefShared = 0x0,  
 cache\_status = FuncCachePreferNone,  
 m\_valid = true,

m\_disabled = false,  
 m\_line\_sz = 128,  
 m\_line\_sz\_log2 = 7,  
 m\_nset = 4,  
 m\_nset\_log2 = 2,  
 m\_assoc = 4,  
 m\_replacement\_policy = LRU,  
 m\_write\_policy = READ\_ONLY,  
 m\_alloc\_policy = ON\_FILL,

m\_mshr\_type = ASSOC,  
 m\_write\_alloc\_policy = NO\_WRITE\_ALLOCATE,  
 {m\_mshr\_entries = 2,  
 m\_fragment\_fifo\_entries = 2},  
 {m\_mshr\_max\_merge = 32,  
 m\_request\_fifo\_entries = 32},  
 {

m\_miss\_queue\_size = 4,  
 m\_rob\_entries = 4},  
 m\_result\_fifo\_entries = 0,  
 m\_data\_port\_width = 128,  
 m\_set\_index\_function = LINEAR\_SET\_FUNCTION},  
 m\_L1T\_config = {

\_vptr.cache\_config = 0x7ffff7da18e0 <vtable for cache\_config+16>,  
 m\_config\_string = 0x62ba50 "4:128:24,  
L:R:m:N:L,  
F:128:4,  
128:2",  
 m\_config\_stringPrefL1 = 0x0,

m\_config\_stringPrefShared = 0x0,  
 cache\_status = FuncCachePreferNone,  
 m\_valid = true,  
 m\_disabled = false,  
 m\_line\_sz = 128,  
 m\_line\_sz\_log2 = 7,  
 m\_nset = 4,  
 m\_nset\_log2 = 2,

m\_assoc = 24,  
 m\_replacement\_policy = LRU,  
 m\_write\_policy = READ\_ONLY,  
 m\_alloc\_policy = ON\_MISS,  
 m\_mshr\_type = TEX\_FIFO,  
 m\_write\_alloc\_policy = NO\_WRITE\_ALLOCATE,  
 {

m\_mshr\_entries = 128,  
 m\_fragment\_fifo\_entries = 128},  
 {m\_mshr\_max\_merge = 4,  
 m\_request\_fifo\_entries = 4},  
 {m\_miss\_queue\_size = 128,  
 m\_rob\_entries = 128},

m\_result\_fifo\_entries = 2,  
 m\_data\_port\_width = 128,  
 m\_set\_index\_function = LINEAR\_SET\_FUNCTION},  
 m\_L1C\_config = {\_vptr.cache\_config = 0x7ffff7da18e0 <vtable for cache\_config+16>,

m\_config\_string = 0x62ba80 "64:64:2,  
L:R:f:N:L,  
A:2:32,  
4",  
 m\_config\_stringPrefL1 = 0x0,  
 m\_config\_stringPrefShared = 0x0,  
 cache\_status = FuncCachePreferNone,  
 m\_valid = true,

m\_disabled = false,  
 m\_line\_sz = 64,  
 m\_line\_sz\_log2 = 6,  
 m\_nset = 64,  
 m\_nset\_log2 = 6,  
 m\_assoc = 2,  
 m\_replacement\_policy = LRU,  
 m\_write\_policy = READ\_ONLY,  
 m\_alloc\_policy = ON\_FILL,

m\_mshr\_type = ASSOC,  
 m\_write\_alloc\_policy = NO\_WRITE\_ALLOCATE,  
 {m\_mshr\_entries = 2,  
 m\_fragment\_fifo\_entries = 2},  
 {m\_mshr\_max\_merge = 32,  
 m\_request\_fifo\_entries = 32},  
 {

m\_miss\_queue\_size = 4,  
 m\_rob\_entries = 4},  
 m\_result\_fifo\_entries = 0,  
 m\_data\_port\_width = 64,  
 m\_set\_index\_function = LINEAR\_SET\_FUNCTION},  
 m\_L1D\_config = {<cache\_config> = {

\_vptr.cache\_config = 0x7ffff7d9ed50 <vtable for l1d\_cache\_config+16>,  
 m\_config\_string = 0x62c220 "32:128:4,  
L:L:m:N:H,  
A:32:8,  
8",  
 m\_config\_stringPrefL1 = 0x7ffff7a7bcd2 "none",

m\_config\_stringPrefShared = 0x7ffff7a7bcd2 "none",  
 cache\_status = FuncCachePreferNone,  
 m\_valid = true,  
 m\_disabled = false,  
 m\_line\_sz = 128,  
 m\_line\_sz\_log2 = 7,  
 m\_nset = 32,

m\_nset\_log2 = 5,  
 m\_assoc = 4,  
 m\_replacement\_policy = LRU,  
 m\_write\_policy = LOCAL\_WB\_GLOBAL\_WT,  
 m\_alloc\_policy = ON\_MISS,  
 m\_mshr\_type = ASSOC,

m\_write\_alloc\_policy = NO\_WRITE\_ALLOCATE,  
 {m\_mshr\_entries = 32,  
 m\_fragment\_fifo\_entries = 32},  
 {m\_mshr\_max\_merge = 8,  
 m\_request\_fifo\_entries = 8},  
 {m\_miss\_queue\_size = 8,

m\_rob\_entries = 8},  
 m\_result\_fifo\_entries = 0,  
 m\_data\_port\_width = 128,  
 m\_set\_index\_function = FERMI\_HASH\_SET\_FUNCTION},  
 <No data fields>},  
 gmem\_skip\_L1D = false,

gpgpu\_dwf\_reg\_bankconflict = false,  
 gpgpu\_num\_sched\_per\_core = 2,  
 gpgpu\_max\_insn\_issue\_per\_warp = 1,  
 gpgpu\_operand\_collector\_num\_units\_sp = 6,

gpgpu\_operand\_collector\_num\_units\_sfu = 8,  
 gpgpu\_operand\_collector\_num\_units\_mem = 2,  
 gpgpu\_operand\_collector\_num\_units\_gen = 0,  
 gpgpu\_operand\_collector\_num\_in\_ports\_sp = 2,

gpgpu\_operand\_collector\_num\_in\_ports\_sfu = 1,  
 gpgpu\_operand\_collector\_num\_in\_ports\_mem = 1,  
 gpgpu\_operand\_collector\_num\_in\_ports\_gen = 0,

gpgpu\_operand\_collector\_num\_out\_ports\_sp = 2,  
 gpgpu\_operand\_collector\_num\_out\_ports\_sfu = 1,  
 gpgpu\_operand\_collector\_num\_out\_ports\_mem = 1,

gpgpu\_operand\_collector\_num\_out\_ports\_gen = 0,  
 gpgpu\_num\_sp\_units = 2,  
 gpgpu\_num\_sfu\_units = 1,  
 gpgpu\_num\_mem\_units = 1,  
 gpgpu\_shader\_registers = 32768,  
 gpgpu\_warpdistro\_shader = -1,

gpgpu\_warp\_issue\_shader = 0,  
 gpgpu\_num\_reg\_banks = 16,  
 gpgpu\_reg\_bank\_use\_warp\_id = false,  
 gpgpu\_local\_mem\_map = true,  
 max\_sp\_latency = 32,  
 max\_sfu\_latency = 512,

n\_simt\_cores\_per\_cluster = 1,  
 n\_simt\_clusters = 15,  
 n\_simt\_ejection\_buffer\_size = 8,  
 ldst\_unit\_response\_queue\_size = 2,  
 simt\_core\_sim\_order = 1,  
 gpgpu\_concurrent\_kernel\_sm = false},

m\_memory\_config = {m\_valid = true,  
 m\_L2\_config = {<cache\_config> = {\_vptr.cache\_config = 0x7ffff7d9ed38 <vtable for l2\_cache\_config+16>,

m\_config\_string = 0x62ad00 "64:128:8,  
L:B:m:W:L,  
A:32:4,  
4:0,  
32",  
 m\_config\_stringPrefL1 = 0x0,  
 m\_config\_stringPrefShared = 0x0,  
 cache\_status = FuncCachePreferNone,  
 m\_valid = true,

m\_disabled = false,  
 m\_line\_sz = 128,  
 m\_line\_sz\_log2 = 7,  
 m\_nset = 64,  
 m\_nset\_log2 = 6,  
 m\_assoc = 8,  
 m\_replacement\_policy = LRU,  
 m\_write\_policy = WRITE\_BACK,

m\_alloc\_policy = ON\_MISS,  
 m\_mshr\_type = ASSOC,  
 m\_write\_alloc\_policy = WRITE\_ALLOCATE,  
 {m\_mshr\_entries = 32,  
 m\_fragment\_fifo\_entries = 32},  
 {m\_mshr\_max\_merge = 4,

m\_request\_fifo\_entries = 4},  
 {m\_miss\_queue\_size = 4,  
 m\_rob\_entries = 4},  
 m\_result\_fifo\_entries = 0,  
 m\_data\_port\_width = 32,  
 m\_set\_index\_function = LINEAR\_SET\_FUNCTION},

m\_address\_mapping = 0x7ffff7dd3a10 <g\_the\_gpu\_config+1136>},  
 m\_L2\_texure\_only = false,

gpgpu\_dram\_timing\_opt = 0x62d150 "nbk=16:CCD=2:RRD=6:RCD=12:RAS=28:RP=12:RC=40: CL=12:WL=4:CDLR=5:WR=12:nbkgrp=4:CCDL=3:RTPL=2",  
 gpgpu\_L2\_queue\_config = 0x7ffff7a7c36d "8:8:8:8",

l2\_ideal = false,  
 gpgpu\_frfcfs\_dram\_sched\_queue\_size = 16,  
 gpgpu\_dram\_return\_queue\_size = 116,  
 scheduler\_type = DRAM\_FRFCFS,  
 gpgpu\_memlatency\_stat = 14,  
 m\_n\_mem = 6,

m\_n\_sub\_partition\_per\_memory\_channel = 2,  
 m\_n\_mem\_sub\_partition = 12,  
 gpu\_n\_mem\_per\_ctrlr = 2,  
 rop\_latency = 120,  
 dram\_latency = 100,  
 tCCDL = 3,  
 tRTPL = 2,  
 tCCD = 2,  
 tRRD = 6,

tRCD = 12,  
 tRCDWR = 7,  
 tRAS = 28,  
 tRP = 12,  
 tRC = 40,  
 tCDLR = 5,  
 tWR = 12,  
 CL = 12,  
 WL = 4,  
 BL = 8,  
 tRTW = 12,  
 tWTR = 11,  
 tWTP = 18,  
 busW = 4,  
 nbkgrp = 4,  
 bk\_tag\_length = 2,

nbk = 16,  
 data\_command\_freq\_ratio = 4,  
 dram\_atom\_size = 64,  
 m\_address\_mapping = {

addrdec\_option = 0x62bb70 "dramid@8;00000000.00000000.00000000.00000000.0000RRRR.RRRRRRRR.BBBCCCCB.CCSSSSSS",  
 gpgpu\_mem\_address\_mask = 1,  
 run\_test = false,  
 ADDR\_CHIP\_S = 8,

addrdec\_mklow = "\000\b\020\000",  
 addrdec\_mkhigh = "@\020\034\r\006",  
 addrdec\_mask = {0,  
 57600,  
 268369920,  
 7935,  
 63},  
 sub\_partition\_id\_mask = 256,  
 gap = 2,  
 m\_n\_channel = 6,

m\_n\_sub\_partition\_in\_channel = 2},  
 icnt\_flit\_size = 32},  
 core\_freq = 700000000,  
 icnt\_freq = 700000000,  
 dram\_freq = 924000000,  
 l2\_freq = 700000000,

core\_period = 1.4285714285714286e-09,  
 icnt\_period = 1.4285714285714286e-09,  
 dram\_period = 1.0822510822510822e-09,  
 l2\_period = 1.4285714285714286e-09,  
 gpu\_max\_cycle\_opt = 0,

gpu\_max\_insn\_opt = 0,  
 gpu\_max\_cta\_opt = 0,  
 gpgpu\_runtime\_stat = 0x62d1c0 "500",  
 gpgpu\_flush\_l1\_cache = false,  
 gpgpu\_flush\_l2\_cache = false,  
 gpu\_deadlock\_detect = true,

gpgpu\_frfcfs\_dram\_sched\_queue\_size = 0,  
 gpgpu\_cflog\_interval = 0,  
 gpgpu\_clock\_domains = 0x62c200 "700.0:700.0:700.0:924.0",  
 max\_concurrent\_kernel = 8,  
 g\_visualizer\_enabled = true,

g\_visualizer\_filename = 0x6211a0 "gpgpusim\_visualizer\_\_Wed-Feb-13-13-30-03-2019.log.gz",  
 g\_visualizer\_zlevel = 6,  
 gpu\_stat\_sample\_freq = 500,  
 gpu\_runtime\_stat\_flag = 0,

liveness\_message\_freq = 1}